REMARKS

Claims 1-25 are pending in the application. Independent claims 1 and 25 have been amended by the present amendment. The amendment is fully supported by the specification as originally filed (see, e.g., page 34, line 1 to page 35, line 14).

Independent claims 1 and 25 have been amended to recite a shift register circuit in which an input control signal of a transfer gate of a corresponding register block is brought into an ON-state only in a specified period when an output of the corresponding flip-flop changes.

Claims 1-3 and 25 were rejected under 35 USC 102(b) as being anticipated by U.S. Patent 5,289,518 to Nakao. The remaining claims were rejected over prior art including the Nakao reference. These rejections are respectfully traversed.

Nakao does not teach or suggest a shift register circuit in which an input control signal of a transfer gate is brought into an ON-state only in a specified period when an output of the corresponding flip-flop changes, as recited in independent claims 1 and 25.

Referring to FIG. 4 of Nakao, the signal N1 is input into a NAND gate 51 along with a clock signal. Therefore, the signal N1 corresponds to an input control signal of the NAND gate 51.

As shown in the timing chart of FIG. 5, the input signal N1 is high **before** the corresponding output signal Q1 of the flip-flop 31 is high. Then, at time T1, when the output signal Q1 of the flip-flop 31 becomes high, the input signal N1 is low.

Therefore, changes in the input signal N1 occur **before** any changes in the output signal Q1 of the flip-flop 31. Further, a change in the output signal Q1 of the flip-flop 31 does not result in the input signal N1 being brought into an ON-state as claimed.

It is noted that the signal CK1 is not an input signal of the NAND gate 51, but instead serves as the output of the NAND gate 51, as shown in FIG. 4.

As amended, claims 1 and 25 require that an **input control signal** of the transfer gate is brought into an ON-state when an output of the corresponding flip-flop changes, which is neither taught nor suggested by the Nakao reference.

For at least the reasons discussed above, the Nakao reference does not anticipate or otherwise render obvious the Applicants' claimed invention.

It is believed that the claims are now in condition for allowance. However, if there are any outstanding issues, the Examiner is urged to call the Applicants' representative at the telephone number listed below.

Respectfully submitted,

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